Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of planarizing a metal layer on a semiconductor substrate, the method comprising:

forming a trench or via in a dielectric layer of the semiconductor substrate;

forming the metal layer on the dielectric layer such that the metal layer at least fills the trenches or vias;

immersing the substrate in an electrolyte plating solution having organic additives, the organic additives comprising at least one of plating accelerators, plating suppressors, and plating levelers; and

planarizing the metal layer by implementing passes of

~~**removing the excess portions of the metal layer by performing sequentially**~~ electropolishing followed by electroplating **wherein the passes begin having ratio of electropolishing rate to electroplating rate that is about 1.5 and as the planarizing continues the ratio of electropolishing rate to electroplating rate for subsequent passes is reduced to a ratio of about one**.

Claim 2 (Original): The method as recited in claim 1, wherein removing the excess portions of the metal layer further comprises a relaxation step after the electropolishing and electrolytic plating steps.

Claim 3 (Original): The method as recited in claim 1 wherein the concentrations of the organic additives are selected such that the plating rate is greater than the electropolishing rate in a topography dependant fashion.

Claim 4 (Original): The method as recited in claim 1 wherein the topography dependant fashion comprises increasing the rate of plating at corners of trenches or vias.

Claim 5 (Original): The method as recited in claim 1 wherein the removal rate of electropolishing is controlled to be equal to that of the electroplating when the polishing exposes the substrate.

Claim 6 (Original): The method as recited in claim 1 wherein the removal rate of electropolishing is controlled by one of adjusting the voltage applied to the electrodes in the electrolytic solution and the duration of the applied voltage.

Claim 7 (Currently Amended): ~~**The method as recited in claim 2**~~ **A method of planarizing a metal layer on a semiconductor substrate, the method comprising:**

forming a trench or via in a dielectric layer of the semiconductor substrate;

forming the metal layer on the dielectric layer such that the metal layer at least fills the trenches or vias;

immersing the substrate in an electrolyte plating solution having organic additives, the organic additives comprising at least one of plating accelerators, plating suppressors, and plating levelers; and

removing the excess portions of the metal layer by performing sequentially electropolishing followed by electroplating, wherein the polishing, plating, and relaxation operations comprise one cycle of a pass and wherein the method comprises at least two passes performed sequentially.

Claim 8 (Original): The method as recited in claim 7 wherein the ratio of the electropolishing to electroplating rates in the first of the at least two passes is about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the at least two passes is about 1.

Claim 9 (Original): The method as recited in claim 7 wherein the ratio of the electropolishing to plating rates in the first of the at least two passes is about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the at least two passes is about 1, wherein the electropolishing to electroplating rates progressively decreases from the first to the last of the at least two passes.

Claim 10 (Original): The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter.

Claim 11 (Original): The method as recited in claim 1 wherein the organic additives comprises a plating suppressor having a concentration in the electrolyte in the range from 5 to 15 ml/liter.

Claim 12 (Original): The method as recited in claim 1 wherein the organic additives comprises a plating leveler having a concentration in the electrolyte in the range from 1 to 5 ml/liter.

Claim 13 (Original): The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter, and a plating suppressor having a concentration in the electrolyte in the range from 5 to 15 ml/liter.

Claim 14 (Original): The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter, a plating suppressor having a concentration in the electrolyte in the range from 1 to 5 ml/liter, and a plating leveler having a concentration in the electrolyte in the range from 1 to 5 ml/liter.

Claim 15 (Original): The method as recited in claim 2 wherein the electropolishing and electroplating is performed using a nozzle configured to spray the wafer and to move form the wafer center to the wafer edge in a pass.

Claim 16 (Original): The method as recited in claim 2 wherein the electropolishing and electroplating is performed using a wafer-wide polisher.

Claim 17 (Original): The method as recited in claim 2 wherein each of the electropolishing, electroplating, and relaxation steps has a duration in the range from 1 to 100 ms.

Claims 18-20 (Cancelled).

Claim 21 (New): A method of planarizing metal on a semiconductor substrate, the method comprising:

providing a semiconductor substrate having a trench or via formed in a dielectric layer of the substrate;

filling the trenches and vias with a metal layer;

spraying the substrate with a coating of electrolyte plating solution having organic additives, the organic additives comprising at least one of plating accelerators, plating suppressors, and plating levelers;

planarizing the metal layer to compensate for excessive trench corner polishing by implementing a series of pulses comprising sequential electropolishing followed by electro plating,

the electropolishing being conducted such that that localized polishing rates inside the trenches at the corners of the trenches are greater than the localized polishing rates in the middle of the trenches resulting in a metal removal profile that removes metal at greater rate at the corner of the trenches relative to a metal removal rate in the middle of the trenches;

the electroplating being conducted such that localized plating rates inside the trenches at the corners of the trenches are greater than the localized plating rates in the middle of the trenches resulting in a metal deposition profile having a thicker metal layer at the corner of the trenches relative to the metal layer in the middle of the trenches; and

the series of pulses being implemented such that the pulses begin with a polishing rate/plating rate ratio of greater than 1 and wherein as the series of pulses continue said ratio decreases to about 1 as the metal layer is planarized to its final profile.

Claim 22 (New): The method as recited in claim 21 wherein in the initial pulse the electropolishing rate/electroplating rate ratio is about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the at least two passes is about 1.

Claim 23 (New): The method as recited in claim 21 wherein the ratio of the electropolishing to plating rates begins at about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the pulses is about 1, wherein the ratio of electropolishing to electroplating rates progressively decreases from the 1.5 to 1.

Claim 24 (New): The method as recited in claim 21 wherein each pulse of sequential electropolishing followed by electroplating further includes a relaxation step.

Claim 25 (New): The method as recited in claim 21 wherein the organic additives include bis (3-sulfopropyl) disulfide.

Claim 26 (New): The method as recited in claim 4 wherein the organic additives include bis (3-sulfopropyl) disulfide.